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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicants: Dominic J. GASBARRO et al.

Serial No.: 09/731,746

Filed: December 8, 2000

For: HOST-FABRIC ADAPTER HAVING BANDWIDTH-OPTIMIZING, AREA-MINIMAL, VERTICAL SLICED MEMORY ARCHITECTURE AND METHOD OF CONNECTING A HOST SYSTEM TO A CHANNEL-BASED SWITCHED FABRIC IN A DATA NETWORK

Art Unit: Unknown

Examiner: Not assigned

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PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, DC 20231

January 17, 2001

Adjustment date: 05/29/2001 TV0111
01/18/2001 HNGUYEN 00000069 09731746
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Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please **add new claims 21-24** as follows:

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--21. A method of storing data consisting of multiple widths and multiple occurrences of data widths in a memory, comprising:

grouping the data widths of the same size and designating as registers;

determining the number of registers;

selecting a number of vertically arranged memory slices of registers of different sizes based on register width and system

architecture requirements such that each memory slice has a number of registers provided by said system architecture and is arranged to supply respective bits of data, via a system bus of said register width requirement;

determining the depth of each of said memory slices based on the respective number of registers provided by said system architecture; and

establishing a default location that is initialized to zero ("0") in all subsequent memory slices which serves as a padding value when a memory location of a respective memory slice exceeding a register width of said memory slice is accessed, via said system bus.

22. The method as claimed in claim 21, wherein said memory is arranged to store context information needed for one or more Micro-Engines (MEs) in a host-fabric adapter to process host data transfer requests for data transfers.

23. The method as claimed in claim **22**, wherein, when a register width requirement is 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12 bits, and 17 registers of 32 bits for a total of 40 registers, said memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into three memory slices, including

Memory C and Memory Z each contains an additional default, last memory location initialized to zero which serves as a padding value to said system bus of 32 bits, when the respective default, last memory location of a respective memory slice is accessed by said Micro-Engine.--

REMARKS

Claims 1-24 are pending in the application. New claims 21-24 are added to alternatively define the process of designing the context memory of the host channel adapter.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 of Antonelli, Terry, Stout & Kraus, LLP (referencing Attorney Docket No. 219.38760X00), and please credit any overpayment of fees to said deposit account.

Respectfully submitted,

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